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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,841	12/12/2003	Lap-Wai Chow	B-4425NP 621267-1	3188

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,841	CHOW ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *7-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Schrantz 4,912,053. Schrantz discloses (see, for example, FIG. 15) a transistor (camouflaged circuit structure) comprising a top gate region (gate region) 130, substrate 120, P-type source region (first active region of a first conductivity type) 140, P-type drain region (second active region of a first conductivity type) 142, and P-type channel region (first well of said first conductivity type) 128. The P-type channel region provides an electrical path between the source and drain regions.

Regarding claim 5, the P-type channel is deeper than the source and drain regions.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 thru 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schrantz '053 as applied to claims 1, and 5 above, and further in view of Spadea 3,983,620. Schrantz

does not disclose a plurality of wells of a second type, at least one of said plurality of wells of a second type being in physical contact with said first active region. However, Spadea discloses (see, for example, Fig. 19) a semiconductor device comprising P+ source and drain regions 17, 17' and N+ guard rings (plurality or wells of a second type) 22. It would have been obvious to one of ordinary skill in the art at the time of invention to have a plurality of wells of a second type, at least one of said plurality of wells of a second type being in physical contact with said first active region in order to isolate the transistor from other elements in a semiconductor device.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schrantz 4,912,053 in view of Maki et al. 6,373,106 B2. Schrantz discloses (see, for example, FIG. 15) a transistor (semiconductor circuit) comprising a substrate 120, top gate region (gate region) 130, P-type source region/drain region (plurality of active regions of a first conductivity type) 140/142, and P-type channel region (first well of said first conductivity type) 128. Schrantz does not disclose a plurality of wells of a second type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second type are separated from said first well. However, Maki discloses (see, for example, FIG. 1) a semiconductor device comprising N-type source/drain regions 4, and P-well (plurality of wells of a second conductivity type) 3b. It would have been obvious to one of ordinary skill in the art at the time of invention to have a plurality of wells of a second type being partially disposed under said at least two of said plurality of active regions, wherein said plurality of wells of a second type are separated from said first well in order to isolate the transistor from other elements in a semiconductor device.

Response to Arguments

6. Applicant's arguments filed 9/2/05 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 8 for claim 1 that the pinchoff voltage of a JFET is a reasonable voltage, this argument is not persuasive. In column 7, lines 48-53, and claim 4, Schrantz discloses that the channel region 128 is formed by implanting impurities, and, therefore, is a discrete, permanent structure in the circuit. Therefore, as the claim is stated (i.e. first well provides an electrical path between said first and second active regions regardless of a reasonable voltage applied to said circuit), the channel region 128 (first well) directly contacts the P-type source region (first active region) 140, and P-type drain region (second active region of a first conductivity type) 142, and definitely provides an electrical path between the regions regardless of a reasonable voltage applied to said circuit. Also, the pinchoff voltage is not the only voltage that can be applied to Schrantz's circuit, and the reasonable voltage stated in the claim may be a different voltage that supports a stronger channel.

Regarding the applicant's argument on page 9 for claim 6 that Maki is limited to a structure comprising at least two transistors of a same conductive type, whereas Schrantz is not limited to such a restrictive feature, this argument is not persuasive. Maki discloses (see, for example, FIG. 1) P-wells (plurality of wells of a second conductivity type) 3b that are partially disposed under N-type source/drain regions (plurality of active regions) 4, and separated from a P-well (first well of said first conductivity type) 3c. The P-wells 3c complement the element isolation regions 2 to isolate a transistor Q2 from another semiconductor device such as transistor

Q1. The function of isolation is not dependent on the conductive type of an adjacent device, and would clearly function as intended (to isolate the transistor) if placed around the transistor of Schrantz.

Regarding the applicant's argument on page 10, first paragraph that Fig. 5 of Maki shows an embodiment wherein P-wells 3b are formed under isolation regions 2 and not in contact with source/drain regions 4, so that "the element separation characteristic may be further improved" and "the semiconductor elements can further be reduced in size", this argument is not persuasive. Even though Maki gives the suggestion that the P-wells may be further improved, it does not deter from the fact that Maki also discloses (see, for example, FIG. 1) another embodiment wherein the P-wells 3b are formed in contact with the source/drain regions 4. Therefore, since Maki clearly discloses P-wells 3b that contact the source/drain regions, and isolate a transistor from another semiconductor device, it would have been obvious to use such an embodiment in Schrantz's invention. There also may be reasons to use the embodiment of FIG. 5 over FIG. 1 that are not expressly disclosed in the specification such as ease of manufacture of producing the P-wells 3b slightly past the element isolation regions 2 versus having the entire P-wells underneath the element isolation regions and not touching the source/drain regions 4.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
October 25, 2005